Low voltage surge protective devices —

Part 21: Surge protective devices connected to telecommunications and signalling networks — Performance requirements and testing methods
National foreword


The start and finish of text introduced or altered by amendment is indicated in the text by tags. Tags indicating changes to IEC text carry the number of the IEC amendment. For example, text altered by IEC amendment 1 is indicated by [3] [4].

Where a common modification to an IEC amendment has been introduced, the tags carry the number of the amendment. For example, the common modifications introduced by CENELEC to IEC amendment 1 are indicated by [5] [6].

The UK participation in its preparation was entrusted by Technical Committee PEL/37, Surge Arresters – High Voltage, to Subcommittee PEL/37/1, Surge arresters – Low voltage.

A list of organizations represented on this subcommittee can be obtained on request to its secretary.

This publication does not purport to include all the necessary provisions of a contract. Users are responsible for its correct application.

Compliance with a British Standard cannot confer immunity from legal obligations.

Amendments/corrigenda issued since publication

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<td>Implementation of IEC amendment 1:2008, with CENELEC modifications</td>
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Low voltage surge protective devices
Part 21: Surge protective devices connected to telecommunications and signalling networks -
Performance requirements and testing methods
(IEC 61643-21:2000 + corrigendum 2001)

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Foreword

The text of document 37A/101/FDIS, future edition 1 of IEC 61643-21, prepared by SC 37A, Low-voltage surge protective devices, of IEC TC 37, Surge arresters, was submitted to the IEC-CENELEC parallel vote and was approved by CENELEC as EN 61643-21 on 2000-11-01.

The following dates were fixed:

- latest date by which the EN has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2002-02-01
- latest date by which the national standards conflicting with the EN have to be withdrawn (dow) 2003-11-01

Endorsement notice

The text of the International Standard IEC 61643-21:2000 + corrigendum March 2001 was approved by CENELEC as a European Standard without any modification.

Foreword to amendment 1

The text of amendment 1:2008 to the International Standard IEC 61643-21:2000, prepared by SC 37A, Low-voltage surge protective devices, of IEC TC 37, Surge arresters, together with common modifications prepared by the Technical Committee CENELEC TC 37A, Low voltage surge protective devices, was submitted to the Unique Acceptance Procedure and was approved by CENELEC as amendment A1 to EN 61643-21:2001 on 2009-03-01.

In this document the common modifications to IEC 61643-21:2000/A1:2008 are indicated by [D] [C].

The following dates were fixed:

- latest date by which the amendment has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2010-03-01
- latest date by which the national standards conflicting with the amendment have to be withdrawn (dow) 2012-03-01

Annex ZA, which was added by CENELEC, has been updated to reflect the changes in the normative references.
Foreword to amendment 2


The following dates are fixed:

- latest date by which the document has to be implemented at national level by publication of an identical national standard or by endorsement (dop) 2013-07-25
- latest date by which the national standards conflicting with the document have to be withdrawn (dow) 2015-08-31

Attention is drawn to the possibility that some of the elements of this document may be the subject of patent rights. CENELEC [and/or CEN] shall not be held responsible for identifying any or all such patent rights.

This standard covers the Principle Elements of the Safety Objectives for Electrical Equipment Designed for Use within Certain Voltage Limits (LVD - 2006/95/EC).

Endorsement notice


In the Bibliography of EN 61643-21:2001, the following note has to be added for the standard indicated:

IEC 60664-1 NOTE Harmonised as EN 60664-1.
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INTRODUCTION

The purpose of this International Standard is to identify the requirements for Surge Protective Devices (SPDs) used in protecting telecommunication and signalling systems, for example, low-voltage data, voice, and alarm circuits. All of these systems may be exposed to the effects of lightning and power line faults, either through direct contact or induction. These effects may subject the system to overvoltages or overcurrents or both, whose levels are sufficiently high to harm the system. SPDs are intended to provide protection against overvoltages and overcurrents caused by lightning and power line faults. This standard describes tests and requirements which establish methods for testing SPDs and determining their performance.

The SPDs addressed in this International Standard may contain overvoltage protection components only, or a combination of overvoltage and overcurrent protection components. Protection devices containing overcurrent protection components only are not within the coverage of this standard. However, devices with only overcurrent protection components are covered in annex A.

An SPD may comprise several overvoltage and overcurrent protection components. All SPDs are tested on a "black box" basis, i.e., the number of terminals of the SPD determines the testing procedure, not the number of components in the SPD. The SPD configurations are described in 1.2. In the case of multiple line SPDs, each line may be tested independently of the others, but there may also be a need to test all lines simultaneously.

This standard covers a wide range of testing conditions and requirements; the use of some of these is at the discretion of the user. How the requirements of this standard relate to the different types of SPD is described in 1.3. Whilst this is a performance standard and certain capabilities are demanded of the SPDs, failure rates and their interpretation are left to the user. Selection and application principles will be covered in IEC 61643-22 1).

If the SPD is known to be a single component device, it has to meet the requirements of the relevant standard as well as those in this standard.

---

1) Under consideration.
LOW VOLTAGE SURGE PROTECTIVE DEVICES –

Part 21: Surge protective devices connected to telecommunications and signalling networks – Performance requirements and testing methods

1 General

1.1 Scope

This International Standard is applicable to devices for surge protection of telecommunications and signalling networks against indirect and direct effects of lightning or other transient overvoltages.

The purpose of these SPDs is to protect modern electronic equipment connected to telecommunications and signalling networks with nominal system voltages up to 1 000 V (r.m.s.) a.c. and 1 500 V d.c.

1.2 SPD configurations

The SPD configurations described in this standard are shown in figure 1. Each SPD configuration is composed of one or more voltage-limiting components and may include current-limiting components.
Figure 1a – Two-terminal SPD

Figure 1b – Three-terminal SPD

Figure 1c – Three-terminal SPD

Figure 1d – Four-terminal SPD

Figure 1e – Five-terminal SPD

Figure 1f – Multi-terminal SPD

Key
V voltage-limiting component
V, I voltage-limiting components or a combination of voltage-limiting and current-limiting components
X1, X2,...Xn line terminals
Y1, Y2,...Yn protected line terminals
C common terminal

Figure 1 – SPD configurations
Table 1 – General SPD requirements

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2 Normative references

The following normative documents contain provisions which, through reference in this text, constitute provisions of this part of IEC 61643. For dated references, subsequent amendments to, or revisions of, any of these publications do not apply. However, parties to agreements based on this part of IEC 61643 are encouraged to investigate the possibility of applying the most recent editions of the normative documents indicated below. For undated references, the latest edition of the normative document referred to applies. Members of ISO and IEC maintain registers of currently valid International Standards.


IEC 60060-1:1989, *High-voltage test techniques – Part 1: General definitions and test requirements*


IEC 60529, *Degrees of protection provided by enclosures (IP code)*


IEC 60950:1999, *Safety of information technology equipment*

IEC 60999-1, *Connecting devices – Electrical copper conductors – Safety requirements for screw-type and screwless-type clamping units – Part 1: General requirements and particular requirements for clamping units for conductors from 0,2 mm² up to 35 mm² (included)*

IEC 61000-4-5, *Electromagnetic compatibility (EMC) – Part 4: Testing and measurement techniques – Section 5 – Surge immunity test*

IEC 61083-1, *Digital recorders for measurements in high voltage impulse tests – Part 1: Requirements for digital recorders*
IEC 61180-1:1992, High-voltage test techniques for low-voltage equipment – Part 1: Definitions, test and procedure requirements

IEC 61643-1, Surge protective devices connected to low-voltage power distribution systems – Part 1: Performance requirements and testing methods

IEC 61643-11:2011, Surge protective devices connected to low-voltage power distribution systems – Part 1: Performance requirements and testing methods

IEC 61643-12:2008, Low-voltage surge protective devices – Part 12: Surge protective devices connected to low-voltage power distribution systems – Selection and application principles


IEC 62305-4:2006, Protection against lightning – Part 4: Electrical and electronic systems within structures

ITU deleted

ITU-T Recommendation K.82, Characteristics and ratings of solid-state, self-restoring overcurrent protectors for the protection of telecommunications installations

ITU-T Recommendation K.44: 2011, Resistibility tests for telecommunication equipment exposed to overvoltages and overcurrents – Basic Recommendation


ITU-T Recommendation O.9:1999, Measuring arrangements to assess the degree of unbalance about earth

3 Definitions

For the purpose of this part of IEC 61643, the following definitions apply.

3.1 model number
code, either applied to the SPD or included in its documentation, that is used to identify the SPD

3.2 preferred values
values for the parameters listed in the tables for the various tests, preferred in the sense that their use promotes uniformity and provides a means of comparison among various protective devices. They also provide a common engineering language beneficial to the user and manufacturer of surge protectors used in telecommunications and signalling networks. However, specific applications may require values other than the preferred values of the tables
3.3 overstressed fault mode
mode 1 condition wherein the voltage-limiting part of the SPD has been disconnected. The
voltage-limiting function is no longer present, but the line is still operable
mode 2 condition wherein the voltage-limiting part of the SPD has been short-circuited by a
very low impedance within the SPD. The line is inoperable, but the equipment is still protected
by a short circuit
mode 3 situation wherein the SPD has undergone an internal open circuit on the network
side of the voltage-limiting part of the SPD. The line is inoperable but the equipment is still
protected by an open line

3.4 protection
application of methods and means to prevent the propagation of stressful electrical energy
beyond a designed interface

3.5 current response time
time required for a current-limiting component to operate at a specified current and a
specified temperature

3.6 maximum continuous operating voltage $U_c$
mmaximum voltage (d.c. or r.m.s.) which may be continuously applied to SPD terminals without
causing any degradation in the transmission characteristics of the SPD

3.7 maximum interrupting voltage
maximum voltage (d.c. or r.m.s.) that can be applied to the current-limiting components of an
SPD without degradation of the SPD. This voltage may be equal to the $U_c$ of the SPD or may
be a higher value depending on the arrangement of the current-limiting component(s) within
the SPD

3.8 surge protective device
SPD
device that restricts the voltage of a designated port or ports, caused by a surge, when it
exceeds a predetermined level

NOTE 1 Secondary functions may be incorporated, such as a current-limiting to restrict a terminal current.
NOTE 2 Typically the protective circuit has at least one non-linear voltage-limiting surge protective component.
NOTE 3 An SPD is a complete assembly, having terminals to connect to the circuit conductors.

3.9 voltage limiting
action of the SPD that causes all voltages exceeding a predetermined value to be reduced

3.10 current limiting
action of an SPD, containing at least one non-linear current-limiting component, that causes
currents exceeding a predetermined value to be restricted
3.11 total discharge current $I_{\text{Total}}$
current which flows through the earthing terminal (common terminal C) of a multi-terminal
SPD during the total discharge current test.

NOTE This may also be called “Total surge current”.

3.12 resettable current limiting
action of an SPD that limits current and can be manually reset after operating

3.13 self-resetting current limiting
action of an SPD that limits current and will self-reset after the disturbing current is removed

3.14 voltage clamping type SPD
SPD that has high shunt impedance and will have a continuous reduction in impedance with
increasing current in response to a voltage surge exceeding the threshold level of the SPD

NOTE Examples of components used in voltage clamping type SPDs: varistors (e.g. MOV) and avalanche
breakdown diodes (ABD).

3.15 voltage switching type SPD
SPD that has a high shunt impedance and will have a sudden and large reduction in
impedance in response to a voltage surge exceeding the threshold level of the SPD

NOTE Examples of components used in voltage switching type SPDs: air gaps, gas discharge tubes (GDT) and
thyristor surge suppressors (TSS).

3.16 voltage protection level $U_p$
parameter that characterizes the performance of the SPD in limiting the voltage across its
terminals. This value of voltage is greater than the highest measured value of impulse-limiting
voltage and is specified by the manufacturer

3.17 multi-stage SPD
SPD which has more than one voltage-limiting component. These voltage-limiting components
may or may not be electrically separated by a series component. The voltage-limiting
components may be either switching or clamping types

3.18 blind spot
situation where voltages above the maximum continuous operating voltage $U_c$ may cause
incomplete operation of the SPD. Incomplete operation of the SPD means not all of the stages
in a multi-stage SPD have operated during the impulse test. This may result in over stressing
of components in the SPD

3.19 a.c. durability
characteristic of an SPD which allows it to conduct alternating current of a specific magnitude
and duration for a specified number of times
3.20 impulse durability
characteristic of an SPD which allows it to conduct impulse current of a specified waveform
and peak value for a specified number of times

3.21 current reset time
time required for a self-resettable current limiter to revert to its normal or quiescent state

3.22 rated current
maximum current a current-limiting SPD can conduct continuously with no change in the
impedance of the current-limiting components

NOTE This is also applicable to linear series components.

3.23 insulation resistance
resistance between designated terminals of an SPD when \( U_c \) is applied to those terminals

3.24 return loss
modulus of the reciprocal of the reflection factor, generally expressed in decibels (dB)

NOTE When impedances can be defined, the return loss in dB is given by the formula:

\[
20 \log_{10} \left( \frac{|Z_s + Z_L|}{|Z_s - Z_L|} \right)
\]

where \( Z_s \) is the characteristic impedance of the transmission line ahead of the discontinuity, or the impedance of
the source, and \( Z_L \) is the impedance after the discontinuity or load impedance seen from the junction between the
source and the load [IEV 702-07-25, modified]

3.25 bit error ratio (BER)
ratio of the number of bit errors to the total number of bits transmitted in a given time interval

3.26 insertion loss
loss resulting from the insertion of an SPD into a transmission system. It is the ratio of the
power delivered to that part of the system following the SPD, before insertion of the SPD, to
the power delivered to that same part after insertion of the SPD. The insertion loss is
generally expressed in decibels [IEV 726-06-07, modified]

3.27 near-end crosstalk (NEXT)
crosstalk that is propagated in a disturbed channel in the direction opposite to the direction of
propagation of the current in the disturbing channel. The terminal of the disturbed channel at
which the near-end crosstalk is present is ordinarily near to, or coincides with, the energized
terminal of the disturbing channel

3.28 longitudinal balance (analogue voice frequency circuits)
electrical symmetry of the two wires comprising a pair with respect to ground
3.29 longitudinal balance (data transmission)
measure of the similarity of impedance to ground (or common) for the two or more conductors of a balanced circuit. This term is used to express the degree of susceptibility to common mode interference

3.30 longitudinal balance (communication and control cables)
ratio of the disturbing common mode (longitudinal) r.m.s. voltage \( V_s \) to ground and the resulting differential mode (metallic) r.m.s. voltage \( V_m \) of the SPD under test, expressed in decibels (dB)
NOTE The longitudinal balance in dB is given by the formula:
\[
20 \log_{10} \frac{V_s}{V_m}
\]
where \( V_s \) and \( V_m \) are measured at the same frequency.

3.31 longitudinal balance (telecommunications)
ratio of the disturbing common mode (longitudinal) voltage \( V_s \) and the resulting differential mode (metallic) voltage \( V_m \) of the SPD under test, expressed in decibels (dB)

3.32 surge (telecommunications)
temporary excessive voltage or current, or both, coupled on a telecommunication line, from an external electrical source
NOTE 1 Typical electrical sources are lightning and AC/DC power systems.
NOTE 2 Electrical source coupling can be one or more of the following: electric, magnetic, electromagnetic, conductive.

3.33 nominal discharge current \( I_n \)
crest value of the current through the SPD having a current waveshape of 8/20

3.34 rated surge current \( I_{SM} \)
maximum value of SPD impulse current with a defined waveshape

3.35 impulse discharge current \( I_{imp} \)
crest value of a discharge current (10/350) through the SPD

4 Service and test conditions

4.1 Service conditions

4.1.1 Normal service conditions

4.1.1.1 Air pressure and altitude
Air pressure is 80 kPa to 106 kPa. These values represent an altitude of +2 000 m to –500 m respectively.

4.1.1.2 Ambient temperature
• normal range: –5 °C to +40 °C
NOTE 1 This range normally addresses SPDs for indoor use. This corresponds to code AB4 in IEC 60364-5-51.
• extended range: −40 °C to +70 °C

NOTE 2 This range normally addresses SPDs for outdoor use in non weather-protected locations, class 3K7 in IEC 60721-3-3.

• storage range: −40 °C to +70 °C

NOTE 3 All values beyond will be specified by the manufacturer.

4.1.1.3 Relative humidity

• normal range: 5 % to 95 %

NOTE 1 This range normally addresses SPDs for indoor use. This corresponds to code AB4 in IEC 60364-5-51.

• extended range: 5 % to 100 %

NOTE 2 This range normally addresses SPDs for outdoor use in non weather-protected locations (e.g. SPD is contained in a weather proofed enclosure).

4.1.2 Abnormal service conditions

Exposure of the SPD to abnormal service conditions may require special consideration in the design or application of the SPD, and shall be called to the attention of the manufacturer.

4.2 Test temperature and humidity

The SPDs shall be tested at a temperature of 25 °C ± 10 °C with relative humidity from 25 % to 75 %.

If required by the manufacturer or customer, the SPDs shall be tested at the extreme temperatures of the service temperature range selected for the intended application. The selected temperature range may be narrower than the full range of 4.1 depending on the application.

For particular SPD technologies, it may be known beforehand that only one of the extreme temperatures of the selected temperature range represents the worst-case test condition. In this case, the testing shall be performed only at the extreme temperature representing the worst-case test condition. This extreme temperature may be different for each test described in clause 6 for the same SPD technology.

When testing is required to be performed at extreme temperatures, SPDs shall be gradually heated or cooled to the specified extreme temperature, taking sufficient time to avoid thermal shock. Unless otherwise specified, a minimum of 1 h should be used. SPDs shall be held at the specified temperature for a time sufficient to reach thermal equilibrium before testing. Unless otherwise specified, a minimum of 15 min should be used.

4.3 SPD testing

The SPDs covered by this standard shall be tested using the connections or terminations that are used when the SPDs are installed in the field. Also, the measurements shall be made at the connections or terminations of the SPDs. For those that are intended to be used with a base or connector, that base or connector shall be part of the tests.

For telecommunication applications ITU-T gives requirements in the K-series for protection holders (K.65) and termination modules (K.55).
When a base is used for testing, the measurements shall be made as close as possible to the terminals of the SPD base (termination module) intended for external connections. Waveform recorders used for measurements shall have a minimum performance in accordance with IEC 61083-1 with respect to the specific measurement.

NOTE For waveform recorders settings, see Annex D.

SPDs of Figures 1c, 1e and 1f may have a common current path (including protective components or just internal connections) that conducts the total impulse current $I_{total}$. The manufacturer shall state the maximum value of impulse current for this current path. This value of impulse current may be less than $n$ times the maximum current capability of each line terminal, where $n$ equals the number of line terminals.

Text deleted

Matters of sample size and permissible failure rates are to be agreed between the customer and manufacturer.

4.4 Waveform tolerances

The definition of the waveform parameters $A/B$ where $A$ is the front time in microseconds and $B$ is the time to half-value in microseconds shall be in accordance with IEC 60060-1 (see also IEC 61000-4-5). Table 2 shows the tolerances for the waveforms used in this standard.

<table>
<thead>
<tr>
<th>Waveform Item</th>
<th>1.2/50 or 10/700 Open-circuit voltage</th>
<th>8/20 or 5/300 Short-circuit current</th>
<th>Other waveforms</th>
</tr>
</thead>
<tbody>
<tr>
<td>Peak</td>
<td>±10 %</td>
<td>±10 %</td>
<td>±10 %</td>
</tr>
<tr>
<td>Front time</td>
<td>±30 %</td>
<td>±20 %</td>
<td>±30 %</td>
</tr>
<tr>
<td>Time to half-value</td>
<td>±20 %</td>
<td>±20 %</td>
<td>±20 %</td>
</tr>
</tbody>
</table>

5 Requirements

5.1 General requirements

The following requirements apply to all SPDs covered by this standard.

5.1.1 Identification and documentation

The information indicated in items a) through n) shall either be marked on the body of the SPD, as described in 5.1.2, or included in the documentation or on the packaging. Any abbreviations used shall be explained in the data sheet. For each test performed on the SPD from clause 6, the test conditions shall be stated in the documentation.
a) Manufacturer's name or trade mark
b) Year and week of manufacture, or serial number
c) Model number
d) Service conditions
e) Maximum continuous operating voltage $U_c$ (AC and/or DC)
f) Rated current
g) Voltage protection level $U_p$
h) Impulse reset (if applicable)
i) AC durability
j) Impulse rating (according to Table 3 - category and corresponding parameters e.g. C2: 2k V/ 1kA)
k) Overstressed fault mode
l) Transmission characteristics (appropriate to the intended SPD use)
m) Additional information, where applicable:
   - replaceable components,
   - the use of radioisotopes,
   - 'I_n' and 'AC overstress current' when impulse overstress test (6.2.1.7) is required
   - surge currents as $I_{SM}$, $I_n$, $I_{imp}$, $I_{Total}$

n) Series resistance (if applicable)
o) (SPD-) Category and rating (if the category is printed on the SPD it is recommended to frame the category in a square. Example: C2)

5.1.2 Marking

The SPDs shall be clearly marked with 5.1.1 items: a) the manufacturer's name or trademark, b) manufacturing traceability, c) model number, and e) the maximum continuous operating voltage. The marking material shall be wipe resistant and resistant to solvents normally used in the SPD application. The location can be under a cover of the enclosure, but shall be easily accessible by the end user (e.g. no tools). Any notes for special handling shall be included in the documentation or on the packaging. Compliance is checked in accordance with 6.1.2.

5.2 Electrical requirements

The SPD shall meet the following requirements when tested in accordance with the subclauses of clause 6.

5.2.1 Voltage-limiting requirements

When the SPD contains only voltage-limiting components, the SPD shall conform to all requirements of 5.2.1. An SPD that contains both voltage-limiting and current-limiting components shall conform to all requirements of 5.2.1 and to all applicable requirements of 5.2.2.

An SPD that contains any linear component between its line terminals and protected line terminals shall conform to the applicable requirements of 5.2.2.
5.2.1.1 Maximum continuous operating voltage ($U_c$)

The manufacturer shall state the maximum continuous operating voltage for the SPD appropriate for the application such as AC rms or DC.

Compliance shall be checked in accordance with 6.2.1.1.

5.2.1.2 Insulation resistance

This characteristic shall be stated by the manufacturer. Compliance shall be checked in accordance with 6.2.1.2.

5.2.1.3 Impulse-limiting voltage

The SPD shall limit a specified impulse voltage when tested at the specified test conditions of table 3. The measured limiting voltage shall not exceed the specified voltage protection level $U_p$. See IEC 61180-1.

5.2.1.4 Impulse reset

This requirement is applicable only to switching-type SPDs. The SPD, after having an impulse wave selected from table 3 applied, shall extinguish or return to its quiescent state. During the application of this impulse wave, a voltage selected from table 4 shall be applied to the SPD. Unless otherwise specified, the SPD shall return to its high impedance state in 30 ms or less.

5.2.1.5 AC durability

The SPD, after having been tested according to 6.2.1.5 using current selected from table 5, shall meet the relevant requirements of 5.2.1 and 5.2.2, if applicable.

5.2.1.6 Impulse durability

The SPD, after having been tested according to 6.2.1.6 using current and voltage waveforms selected from table 3, shall meet the relevant requirements of 5.2.1 and 5.2.2, if applicable.

5.2.1.7 Overstressed fault mode

The SPD shall not become a fire hazard, explosion hazard or electrical hazard and shall not emit toxic fumes when tested in accordance with 6.2.1.7.

The manufacturer shall provide the value of the impulse current (B/20) and the value of alternating current which will lead to a fault mode as described in 6.2.1.7.

5.2.1.8 Blind spot

If no information regarding blind spots is available from the manufacturer, or verification of the manufacturer's information is desired, the testing of multi-stage SPDs shall be performed as described in 6.2.1.8.

5.2.2 Current-limiting requirements

When the SPD contains a combination of both voltage-limiting and current-limiting components, the current-limiting components shall conform to all applicable requirements of 5.2.2. An SPD that contains a linear component (for example, resistor, inductor) between its line terminals shall conform to the requirements of 5.2.2.1, 5.2.2.2, 5.2.2.7 and 5.2.2.8.
5.2.2.1 Rated current

The manufacturer shall specify the rated current. To confirm this value of rated current, the SPD shall be tested according to 6.2.2.1. Application of this test shall cause no change in the operating characteristics of the current-limiting component of the SPD.

5.2.2.2 Series resistance

The manufacturer shall specify the value and tolerance of any series resistance. To confirm this value of series resistance, the SPD shall be tested according to 6.2.2.2.

5.2.2.3 Current response time

When tested according to 6.2.2.3, the current-limiting component(s) shall operate at or below the value of response time specified by the manufacturer. Preferred values of test current are given in table 6. See ITU-T Recommendation K.30.

5.2.2.4 Current reset time

The SPD containing one or more self-resettable current-limiting components shall be tested in accordance with 6.2.2.4. The reset time, or time required for the current-limiting component(s) to return to their quiescent state, shall be less than 120 s, unless otherwise specified.

This requirement is not applicable to SPDs containing manually resettable current-limiting component(s).

5.2.2.5 Maximum interrupting voltage

This requirement is applicable only to SPDs containing self-resettable or manually resettable current-limiting component(s). The SPD manufacturer shall specify the maximum interrupting voltage of the current-limiting component(s) in the SPD. Confirmation of this value is determined by performing the test in 6.2.2.5. There shall be no degradation in the operating characteristics of the current-limiting components after this test.

5.2.2.6 Operating duty test

This requirement is applicable only to SPDs containing self-resettable or manually resettable current-limiting component(s). The SPD shall be subjected to repeated applications of the maximum interrupting voltage. The current shall be sufficient to operate the current-limiting component(s) and shall be selected from table 7. After exposure to these tests, the current-limiting component(s) shall meet the requirements of 5.2.2.3 and 5.2.2.4.

5.2.2.7 AC durability

The SPD shall be subjected to repeated applications of a specified current. Table 8 shows preferred values of alternating currents. After exposure to these currents, the current-limiting component(s) in the SPD shall meet the requirements of 5.2.2.1, 5.2.2.2 and 5.2.2.3.
5.2.2.8 Impulse durability

The SPD shall be subjected to a specified number of surges of specified peak current. Table 9 shows preferred values. After application of these surges in accordance with 6.2.2.8, the current-limiting component(s) of the SPD shall meet the requirements of 5.2.2.1, 5.2.2.2 and 5.2.2.3.

5.2.3 Transmission requirements

The SPD, in addition to the requirements of 5.2.1 and 5.2.2, may need to conform to specific requirements of 5.2.3 depending on its communication and signalling application (for example, voice, data, and video). Table 1 provides guidance in the selection of applicable transmission tests.

5.2.3.1 Capacitance

The manufacturer shall state the value of capacitance between specified terminals. Confirmation shall be determined by testing in accordance with 6.2.3.1.

5.2.3.2 Insertion loss

The SPD shall be tested in accordance with 6.2.3.2 to determine whether the insertion of the SPD into the test system results in a voltage reduction between the generating and the measuring equipment.

5.2.3.3 Return loss

The SPD shall be tested in accordance with 6.2.3.3. This will determine the amount of signal reflected back to the signal source, over a specified frequency range, caused by the insertion of the SPD into a matched transmission line.

5.2.3.4 Longitudinal balance

The SPD shall be tested in accordance with 6.2.3.4. This test determines the minimum acceptable level of longitudinal balance of an SPD used in balanced circuits. The longitudinal balance shall be measured in the frequency range of interest.

5.2.3.5 Bit error ratio (BER)

The SPD shall be tested in accordance with 6.2.3.5. This test determines whether the insertion of a surge protective device causes bit errors in a digital transmission system.

5.2.3.6 Near-end crosstalk (NEXT)

The SPD shall be tested in accordance with 6.2.3.6. This test determines the amount of signal that is coupled from one circuit to another due to the insertion of the SPD.

5.3 Mechanical requirements

The SPD shall conform to the following mechanical requirements. However, certain mechanical requirements may be superseded by national regulations.
5.3.1 Terminals and connectors

a) Terminals and connectors shall be fastened to the SPD in such a way that they will not work loose if the clamping screws or the lock-nuts are tightened or loosened. A tool shall be required to loosen the clamping screws or the lock-nuts.

b) Screws, current-carrying parts and connectors

1) Connections, whether electrical or mechanical, shall withstand the mechanical stresses occurring in normal use, and the mechanical stresses generated by high current surges.

Screws operated when mounting the SPD during installation shall not be of the thread-cutting type.

Compliance is checked by inspection and tested in accordance with 6.3.1.2.

2) Electrical connections shall be so designed that contact pressure is not transmitted through insulating material other than ceramic, pure mica or other material with characteristics no less suitable, unless there is sufficient resilience in the metallic parts to compensate for any possible shrinkage or yielding of the insulating material.

Compliance is checked by inspection.

The suitability of the material is considered with respect to the dimensions.

3) Current-carrying parts and connections including parts intended for grounding conductors, if any, shall be of

- copper, or
- an alloy containing at least 58% copper for cold-worked parts, or
- an alloy containing at least 50% copper for non-cold-worked parts, or other metal or suitably coated metal, no less resistant to corrosion than copper and having mechanical properties no less suitable.

Requirements for mechanical connections for specific terminals are covered in IEC 61643-1.

c) Screwless terminals for external conductors

1) Terminals shall be so designed and constructed that

- each conductor is clamped individually and the conductors can be connected or disconnected either at the same time or separately;
- it is possible to clamp securely any number of conductors up to the maximum provided.

2) Terminals shall be so designed and constructed that they clamp the conductor without undue damage to the conductor.

Compliance is checked by inspection.

d) Insulation pierced connections for external conductors

1) The insulation pierced connections shall make a reliable mechanical connection.

Compliance is checked by inspection and tested in accordance with 6.3.1.4.

2) Screws for making contact pressure shall not serve to fix any other component, although they may hold the SPD itself in place or prevent it from turning.

Compliance is checked by inspection.

3) Screws shall not be of metal which is soft or liable to creep.

Compliance is checked by inspection.

e) Corrosion resistant metals

Clamps (except clamping screws), lock-nuts, binding clips, thrust washers, wire, and similar parts, shall consist of corrosion resistant metal (see IEC 60999-1).
5.3.2 Mechanical strength (mounting)
SPDs shall be provided with appropriate means for mounting that will ensure mechanical stability.

5.3.3 Resistance to ingress of solid objects and to harmful ingress of water
SPDs shall be designed in such a way that they operate satisfactorily under the service conditions described in 4.1. SPDs installed in the outdoor environment shall be contained in a weather shield of glass, glazed ceramic or other acceptable material that is resistant to UV radiation, corrosion, erosion, and tracking.

They shall have sufficient surface creepage distance between any two parts of different potential. In some countries, other national regulations may apply.

5.3.4 Protection against direct contact
For protection against direct contact (inaccessibility of live parts), SPDs shall be designed in such a way that live parts cannot be touched when the SPD is installed for the intended use. This requirement is valid for accessible SPDs where the $U_c$ is above 50 V r.m.s. or 71 V d.c.

SPDs, except SPDs classified as inaccessible, shall be so designed that, when they are wired and mounted as for normal use, live parts are not accessible, even after removal of parts which can be removed without the use of a tool (checked by the isolated parts test of 6.3.4).

The connection between the grounding terminals, and all accessible parts connected thereto, shall be of low resistance (see IEC 60529).

In some countries, other national regulations may apply.

5.3.5 Fire resistance
Insulating parts of the housing shall be either non-flammable or self-extinguishing.

In some countries, other national regulations may apply.

5.4 Environmental requirements
The SPD intended only for the uncontrolled environment of 4.1, shall conform to the following environmental requirements after an agreement between the user and the manufacturer.

5.4.1 High temperature and humidity endurance
The SPD shall be exposed to 80 °C and 90 % RH. The duration of the exposure shall be selected from table 15. This test shall be performed only on those SPDs intended for use in uncontrolled environments, and shall be in accordance with 6.4.1. After exposure, the voltage-limiting component(s) of the SPD shall meet the requirements of 5.2.1.2 and 5.2.1.3. If the SPD under test contains current-limiting component(s), these shall meet the requirements of 5.2.2.2 and 5.2.2.3.

If a manufacturer's series of SPDs are identical, except for the $U_c$ value, and the parts used are identical, except changes in the voltage ratings of voltage-limiting and current-limiting components to match a specific SPD $U_c$ value, then only the SPD with the highest voltage protection level shall be tested.
5.4.2 Environmental cycling with impulse surges

The SPD shall be subjected to temperature cycling at high humidity while conducting impulse currents. The type of temperature cycling shall be selected from table 16.

During and after cycling, the voltage-limiting component(s) of the SPD shall meet the requirements of 5.2.1.2 and 5.2.1.3. If the SPD under test contains current-limiting component(s), these shall meet the requirements of 5.2.2.2 and 5.2.2.3.

This test shall be performed only on those SPDs intended for use in uncontrolled environments, and shall be performed in accordance with 6.4.2.

If a manufacturer’s series of SPDs are identical, except for the $U_c$ value, and the parts used are identical, except changes in the voltage ratings of voltage-limiting and current-limiting components to match a specific SPD $U_c$ value, then only the SPD with the highest voltage protection level shall be tested.

5.4.3 Environmental cycling with a.c. surges

The SPD shall be subjected to temperature cycling at high humidity while conducting alternating currents. These currents and their duration shall be selected from table 5. The type of temperature cycling shall be selected from table 16.

During and after cycling, the SPD shall meet the requirements of 5.2.1.2 and 5.2.1.3.

This test shall be performed only on those SPDs intended for use in uncontrolled environments and shall be performed in accordance with 6.4.3.

If a manufacturer’s series of SPDs are identical, except for the $U_c$ value, and the parts used are identical, except changes in the voltage ratings of voltage-limiting and current-limiting components to match a specific SPD $U_c$ value, then only the SPD with the highest voltage protection level shall be tested.

6 Type test

6.1 General tests

6.1.1 Identification and documentation

Identification and documentation shall meet the requirements of 5.1.1 by inspection.

6.1.2 Marking

Verification of the markings shall be carried out by inspection. The following indelibility test shall be applied on markings of all types except those made by impressing, moulding and engraving.

The test is made by rubbing the marking by hand for 15 s with a piece of cotton wool soaked with water and again for 15 s with a piece of cotton soaked with hexane solvent with a content of aromatics of maximum 0.1 % volume, a kauributanol value of 29, initial boiling-point approximately 65 °C and specific gravity of 0.68 g/cm³. After this test, the marking shall be easily legible.
6.2 Electrical tests

6.2.1 Voltage-limiting tests

If not otherwise specified, for all tests where a power supply at \( U_C \) or at the maximum interrupting voltage is required, the voltage tolerance for testing shall be \( \pm 0.5 \% \). When DC is used the maximum ripple shall not exceed 5 \%. When AC is used tests shall be performed at 50 Hz or 60 Hz, except if otherwise specified by the manufacturer.

At all voltage-limiting tests it is required to test the common mode (X1-C, X2-C). Testing of the differential mode (X1-X2) is optional.

NOTE Basic configurations for measuring \( U_p \) are listed in informative Annex F.  

6.2.1.1 Maximum continuous operating voltage (\( U_C \))

\( U_C \) shall be verified during the insulation resistance test in 6.2.1.2.

6.2.1.2 Insulation resistance

Insulation resistance shall be measured in both polarities at one pair of terminals at a time. The test voltage shall be equal to \( U_C \). If \( U_C \) of the SPD has AC and DC values, this device shall be tested with both AC and DC. If \( U_C \) of this SPD has only an AC value this device shall be tested with DC. At this the DC voltage is calculated as \( U_{dc} = U_{ac} \times \sqrt{2} \). For polarised (polarity dependent) constructions of DC SPDs the test shall be carried out in one polarity only. The current conducted between the tested terminals shall be measured.

The insulation resistance is equal to the applied test voltage at the device terminals divided by the measured current and shall be higher than or equal to the value stated by the manufacturer.

6.2.1.3 Impulse-limiting voltage

The SPDs shall be tested using one impulse selected from category C of Table 3 and applied to the appropriate terminals. The current level shall be selected based on the current carrying capability of the SPD as determined in the impulse durability test (see 6.2.1.6). Both impulse-limiting voltage and impulse durability tests shall be performed with the same impulse. Values listed in Table 3 are minimum requirements, other surge current ratings can be found in standards e.g. ITU-T K. series recommendations.

NOTE 1 Testing of the Impulse limiting voltage \( "U_p" \) is not necessary for test categories A, B and D.

Text deleted

Apply five negative and five positive impulses. The generator used shall have its open-circuit voltage and short-circuit current selected from Table 3.
Measure the voltage limitation for each impulse without load. The maximum voltage measured at the appropriate terminals shall not exceed the specified voltage protection level \( (U_p) \). Sufficient time shall be allowed between impulses to prevent accumulation of heat. It is understood that different SPDs will have different thermal characteristics, and consequently will require different times between impulses.

**NOTE 2** Detailed information about impulse recorder settings can be found in Annex D.

If it is required, the impulse may be applied to terminals X1 – X2 of SPDs shown in figures 1c) and 1e).

For tests on the SPDs shown in figures 1c) and 1e), each pair of terminals (X1 – C and X2 – C) may be tested at the same time and same polarity, or separately.

For SPDs that have a common current path (refer to 4.3), the voltage on the line terminals where no impulse is applied shall be measured during the test and shall not exceed \( U_p \).
### Table 3 – Voltage and current waveforms for impulse-limiting voltage and impulse durability

<table>
<thead>
<tr>
<th>Category</th>
<th>Type of test</th>
<th>Open-circuit voltage *</th>
<th>Short-circuit current</th>
<th>Minimum number of applications</th>
<th>Terminals to be tested</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>Very slow rate of rise</td>
<td>≥ 1 kV</td>
<td>10 A, ≥ 1,000 μs</td>
<td>Not applicable (NA)</td>
<td>X1 – C X2 – C X1 × X2</td>
</tr>
<tr>
<td>A2</td>
<td>AC</td>
<td>Select a test from Table 5</td>
<td>Single cycle</td>
<td></td>
<td></td>
</tr>
<tr>
<td>B1</td>
<td>Slow rate of rise</td>
<td>1 kV 10/1000</td>
<td>100 A, 10/1000</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td>B2</td>
<td>Slow rate of rise</td>
<td>1 kV to 4 kV 10/700</td>
<td>25 A to 100 A 5/320</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td>B3</td>
<td>Slow rate of rise</td>
<td>≥ 1 kV 100 V/μs</td>
<td>10 A to 100 A 10/1000</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td>C1</td>
<td>Fast rate of rise</td>
<td>0.5 kV to 2 kV 1.2/50</td>
<td>0.25 kA to 1 kA 8/20</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td>C2</td>
<td>Fast rate of rise</td>
<td>2 kV to 10 kV 1.2/50</td>
<td>1 kA to 5 kA 8/20</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>C3</td>
<td>Fast rate of rise</td>
<td>≥ 1 kV 1 kV/μs</td>
<td>10 A to 100 A 10/1000</td>
<td>300</td>
<td></td>
</tr>
<tr>
<td>D1</td>
<td>High energy</td>
<td>≥ 1 kV</td>
<td>0.5 kA to 2.5 kA 10/350</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>D2</td>
<td>High energy</td>
<td>≥ 1 kV</td>
<td>0.6 kA to 2.0 kA 10/250</td>
<td>5</td>
<td></td>
</tr>
</tbody>
</table>

* An open-circuit voltage different from 1 kV may be used as long as the SPD under test operates.

** X1 – X2 terminals are tested only if required.

For the verification of $U_p$, only one impulse waveform of category C is mandatory. Apply 5 positive and 5 negative impulses.

For impulse durability measurement, one impulse waveform of category C is mandatory and A1, B and D are optional.

B1, B2, C1, C2 and D2 are voltage driven tests and therefore the column “Short-circuit current” shows the prospective short-circuit current at the DUT connection point. Categories B3, C3 and D1 are current driven tests, therefore the required test current is adjusted through the DUT. The max. waveform tolerances as listed in table 2 shall not be exceeded. For the voltage driven tests the effective output impedance of the generators used shall be 10 Ohms for Category B1, 40 Ohms for Category B2 and 2 Ohms for Categories C1, C2 and D2.

NOTE Values listed in Table 3 are minimum requirements.

* Text and figure deleted��息内容
6.2.1.4 **Impulse reset**

The SPD shall be connected as shown in Figure 2. The impulse reset voltage and current values shall be taken from the manufacturer's datasheet or shall be based on the voltage/current combinations listed in Table 4 following the manufacturer's instructions. These power sources represent commonly used system values. AC SPDs have to be tested with AC, DC SPDs have to be tested with DC, and AC/DC SPDs have to be tested with DC. Depending on the construction of DC SPDs the test can be carried out only in one polarity. If an AC test is performed the impulse generator must be synchronized with the phase of the AC voltage (typically at a phase angle between $30^\circ$ and $60^\circ$).

For the impulse voltage and current waveform either Category B1 or C1 shall be selected from Table 3. The peak open-circuit voltage shall be sufficient to ensure that the voltage-switching component(s) of the SPD operates. The polarity of the impulse voltage shall be the same as the polarity of the voltage source. The reset time is defined as the time from application of the impulse to the return of the SPD to its high-impedance state.

One positive and one negative impulse shall be applied at an interval not greater than 1 min, and the reset time shall be measured for each impulse.

**NOTE** The polarity of the diodes in a decoupling device (figure 2) must be reversed when the polarity of the DC power supplies and surge generator are reversed.

<table>
<thead>
<tr>
<th>Table 4 – Source voltages and currents for impulse reset test</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Open-circuit source voltage</strong> &amp; <strong>Short-circuit source current</strong></td>
</tr>
<tr>
<td>V</td>
</tr>
<tr>
<td>---</td>
</tr>
<tr>
<td>12</td>
</tr>
<tr>
<td>24</td>
</tr>
<tr>
<td>48</td>
</tr>
<tr>
<td>97</td>
</tr>
<tr>
<td>135</td>
</tr>
</tbody>
</table>

a The SPD may be connected in parallel by a series combination of a 135-150 Ω resistor and a 0.08 μF to 0.1 μF capacitor.

b Tolerance (including ripple) +/- 1% c

6.2.1.5 **AC durability for voltage limiting function**

The SPD shall be connected as shown in Figure 3. The AC short-circuit current shall be selected from Table 5. Apply the currents for the specified number of applications with time between applications sufficient to prevent accumulation of heat in the device under test. The applied AC test voltage shall be of sufficient magnitude to cause a full conduction of the voltage limiting component(s) of the SPD. Prior to testing and after completion of the required number of AC applications, the SPD shall meet the requirements of 5.2.1.2, 5.2.1.3, 5.2.1.4 (if applicable) and 5.2.2.2.
The currents, selected from table 5, shall be applied to the appropriate terminals.

If required by the manufacturer or customer, the currents may be applied additionally to terminals X1 – X2 of SPDs shown in figures 1c), 1e) and 1f).

For tests on the SPDs shown in figures 1c), 1e) and 1f), each pair of terminals (X1 – C and X2 – C) may be tested separately.

For SPDs that have a common current path, refer to 4.3. Otherwise, for multi-terminal SPDs test each line terminal to common terminal separately.

Table 5 – Preferred values of currents for a.c. durability test

<table>
<thead>
<tr>
<th>48 Hz-62 Hz Short-circuit currents on each tested terminal a</th>
<th>Duration</th>
<th>Number of applications b</th>
<th>Test terminals</th>
</tr>
</thead>
<tbody>
<tr>
<td>A_rms</td>
<td>s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>0,1</td>
<td>1</td>
<td>5</td>
<td>X1 – C</td>
</tr>
<tr>
<td>0,25</td>
<td>1</td>
<td>5</td>
<td>X2 – C</td>
</tr>
<tr>
<td>0,5</td>
<td>1</td>
<td>5</td>
<td>X1 – X2 c</td>
</tr>
<tr>
<td>0,5</td>
<td>30</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>60</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>2,5</td>
<td>1</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>1</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>20</td>
<td>1</td>
<td>5</td>
<td></td>
</tr>
</tbody>
</table>

a Values listed in Table 5 are minimum requirements.

b Different numbers of applications can be found in other standards e.g. ITU-T K series – Recommendations.

c X1 – X2 terminals shall be tested only if required.

6.2.1.6 Impulse durability for voltage limiting function

The SPD shall be tested using one impulse selected from Category C of table 3 and applied to the appropriate terminals selected from table 3. The same impulse shall be used to perform the impulse-limiting voltage test in 6.2.1.3. Additional tests may be performed using other impulses selected from Categories A1, B, C and D as well as those listed in the SPD documentation. However, these tests are optional and should only be used as appropriate to the application of the SPDs.

The SPD shall be connected as shown in figure 4. Apply the impulse current for the minimum number of applications specified in table 3 with time between applications sufficient to prevent accumulation of heat in the device under test. Half the specified number of tests shall be carried out with one polarity followed by half with the opposite polarity. Alternatively, half of the samples may be tested with one polarity and the other half with the opposite polarity. Prior to testing and after the completion of the number of applications, the SPD shall meet the requirements of 5.2.1.2, 5.2.1.3 (one impulse each polarity), 5.2.1.4 (if applicable) and 5.2.2.2 (if applicable).
If required, the impulse may be applied to terminals X1 – X2 of SPDs shown in figures 1c) and 1e).

For tests on the SPDs shown in Figures 1c) and 1e), each pair of terminals (X1 – C and X2 – C) may be tested separately. For tests on the SPD shown in Figure 1f) it is sufficient to select two terminals as a representative sample, provided all terminals have the same protective circuit to terminal C.

Text deleted

6.2.1.6.1 Additional test for Multi-terminal SPDs

If the manufacturer declares a total impulse current the test according 6.2.1.6 shall be repeated with the following modification and additions.

This test is not required if the SPD’s total impulse current capability is equal to the single line impulse current capability (e.g. total impulse current = 10 kA, single line impulse current = 10 kA).

Multi-terminal SPDs (fig. 1c, 1f, 1e) may have the total impulse current (I_{total}) flowing through common components and connections to the earthing terminal. Two examples are shown in Figure 16. All the protected lines shall have an impulse current equal to the total impulse current divided by the number of lines, applied simultaneously to verify that the common current path has sufficient current capability. After this test the SPD shall not be degraded. This test also verifies that the internal connections of the SPD have sufficient current capability.

The coupling network shall not substantially influence the test impulse. The permissible deviation from the 8/20 waveform of the test impulse for categories C1 and C2 shall not exceed an 8/25 waveform with a tolerance of +/- 30% for both the front time and the time to half value.

NOTE If it is not possible to reach the above waveform parameters the test may be performed with modified SPDs provided by the manufacturer, where every “individual protective element” (1) of the star protection circuit shown in Figure 16 is short circuited. During the test all input terminals X1 to Xn are connected together.

6.2.1.7 Overstressed fault mode

The SPD shall be overstressed by impulse overstress and a.c. overstress currents. For tests on the SPDs shown in Figures 1c, 1e and 1f, each pair of terminals (X1 – C and X2 – C) may be tested separately. For SPD 1f select two terminals as a representative sample. Different SPDs shall be tested for impulse and a.c. tests.

Insulation resistance, voltage-limiting and series resistance tests shall be performed as applicable to determine if the SPD has reached an acceptable overstressed fault mode as described in 3.3. The SPD shall reach its overstressed fault mode in a safe manner without causing a fire hazard, an explosion hazard, an electrical hazard or emission of toxic fumes.

NOTE 1 For multistage SPDs different fault modes are allowed. (e.g. X1 - C could have a mode 2 and the X1 – X2 could have mode 1)
Impulse overstress

The SPD shall be connected as shown in figure 4. The 8/20 impulse current, $i_n$, specified by the manufacturer shall be applied to the SPD in the following manner:

$$i_{test} = i_n (1 + 0.5 N)$$

The test sequence shall begin with $N = 0$ ($i_{test} = i_n$). For each subsequent test, $N$ increases by 1. This sequence is limited to $N = 6$. If the SPD does not reach an overstressed fault mode after these applications, the SPD shall be tested for overstressed fault mode with a.c.

NOTE 2 If $i_n$ exceeds the capability of the hybrid generator a pure 8/20 current generator shall be used. The peak current flowing through the SPD shall be adjusted to the value of the specified and calculated surge current $i_n$.

AC overstress

The SPD shall be connected as shown in Figure 3. The AC overstress current shall be specified by the manufacturer. The current shall be applied for 15 min. The open-circuit voltage, 50 Hz or 60 Hz, shall have sufficient magnitude to cause a full conduction of the SPD.

NOTE 3 The adjusted test current is the short-circuit current of the source.

6.2.1.8 Blind spot test

In order to determine whether blind spots exist in a multi-stage SPD, the following tests using a new sample shall be performed.

a) Select the same impulse waveform used to determine $U_c$ (see 6.2.1.3). During the application of this impulse, measure the impulse-limiting voltage and the voltage-time waveform with an oscilloscope.

b) Reduce the open-circuit voltage to 10 % of the value used in a), and apply one positive impulse to the SPD while monitoring the limiting voltage with an oscilloscope. The limiting voltage waveform should be different from that obtained in a). If it is not, select a lower open-circuit voltage. However, this voltage shall be above $U_c$.

c) Apply positive impulse voltages whose values are 20 %, 30 %, 45 %, 60 %, 75 % and 90 % of the value used in a), while continuing to monitor the limiting voltage waveform.

d) At the open-circuit voltage percentage when the limiting voltage waveform returns to that as determined in a), stop.

e) Reduce the open-circuit voltage by 5 % and retest. Continue reducing the open-circuit voltage in steps of 5 % until the waveform noted in b) is obtained.

f) At this value of open-circuit voltage, apply two impulses of positive polarity and two impulses of negative polarity.

After testing a) through f), the SPD shall meet the requirements of 5.2.1.2.

6.2.2 Current-limiting tests

6.2.2.1 Rated current

The SPD shall be connected as shown in Figure 5. The source capability shall be sufficient to supply the rated current. The frequency shall be 0 (DC) or 50 Hz or 60 Hz. AC SPDs have to be tested with AC, DC SPDs have to be tested with DC, and AC/DC SPDs have to be tested with DC.
During the rated current tests the current-limiting function, if present, shall not operate. For each SPD configuration, the test current shall be applied by adjusting the $R_s$, or $R_{s1}$ and $R_{s2}$ resistances. The current-limiting function under test shall conduct the rated current for a 1 h minimum period. During this test the touchable parts shall not reach excessive temperatures (see 4.5.1 of IEC 60950).

### 6.2.2.2 Series resistance

The SPD shall be connected as shown in Figure 5. The test source voltage shall be $U_c$. The frequency shall be 0 (DC) or 50 Hz or 60 Hz. AC SPDs have to be tested with AC, DC SPDs have to be tested with DC, and AC/DC SPDs have to be tested with DC. 

The test current shall be made equal to the rated current by adjusting the $R_s$, or $R_{s1}$ and $R_{s2}$ resistances. The resistance is determined by $(e - IR_s)/i$ where $e$ is the source voltage and $i$ is the rated current as measured by the ammeter in figure 5.

### 6.2.2.3 Current response time

The SPD shall be connected as shown in Figure 5. The source voltage shall be $U_c$. The frequency shall be either 0 Hz (DC) or 50 Hz or 60 Hz AC SPDs have to be tested with AC, DC SPDs have to be tested with DC, and AC/DC SPDs have to be tested with DC.

Devices shall be tested at appropriate temperatures with reference to 4.2. Sufficient time shall be allowed between tests to ensure that devices cool back to testing temperature prior to subsequent testing. Alternatively, separate devices can be used for each test to avoid waiting for the cooling period. $R_s$ or $R_{s1}$ and $R_{s2}$ shall be set to provide the desired prospective test currents of Table 6. The response time of the current-limiting function at each test current shall be recorded. The response time is the time from application of power until the current falls to 10 % of the rated current. If the prospective test current exceeds the maximum current capability of the current-limiting component(s), then the highest test current shall be the maximum current capability of the current-limiting component(s).

### Table 6 - Test currents for response time

<table>
<thead>
<tr>
<th>Test currents</th>
<th>A</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5× rated current</td>
<td>A</td>
</tr>
<tr>
<td>2.1× rated current</td>
<td>A</td>
</tr>
<tr>
<td>2.75× rated current</td>
<td>A</td>
</tr>
<tr>
<td>4.0× rated current</td>
<td>A</td>
</tr>
<tr>
<td>10.0× rated current</td>
<td>A</td>
</tr>
</tbody>
</table>

### 6.2.2.4 Current reset time

The SPD shall be connected as shown in Figure 5. The source voltage shall be $U_c$. The frequency shall be 0 (DC), 50 Hz or 60 Hz. AC SPDs have to be tested with AC, DC SPDs have to be tested with DC, and AC/DC SPDs have to be tested with DC.
For each SPD configuration, the initial load current shall be the rated current, obtained by adjusting the \( R_0 \), or \( R_{81} \) and \( R_{82} \) resistances. The SPD shall be allowed to stabilize at the rated current. After the stabilization, the \( R_0 \), or \( R_{81} \) and \( R_{82} \) resistances shall be reduced to values such that the load current increases to a level that causes the current-limiting function of the SPD to operate. This test condition shall be maintained for 15 min after the current is reduced below 10 % of the rated current.

The \( R_0 \), or \( R_{81} \) and \( R_{82} \) resistances shall then be increased to their initial values. The time which it takes for the load current to return to at least 90 % of the rated current, shall be recorded and shall be less than 120 s. Depending on the application, testing may be done at currents lower than the rated current for self-resetting current-limiting functions. For resettable current-limiting components, the source current shall be interrupted for a time of less than 120 s. After this, the resettable current-limiting function shall conduct the rated current for a period of 5 min to ensure that the current-limiting function has reverted to its quiescent state.

6.2.2.5 Maximum interrupting voltage

The SPD shall be connected as shown in Figure 5. The test voltage shall be the maximum interrupting voltage as specified by the manufacturer. The frequency shall be 0 (DC) or 50 Hz or 60 Hz. AC SPDs have to be tested with AC, DC SPDs have to be tested with DC, and AC/DC SPDs have to be tested with DC.

The \( R_0 \), or \( R_{81} \) and \( R_{82} \) resistances shall be adjusted to a value that causes the operation of the current-limiting component of the SPD. This test condition shall be maintained for 1 h. After 1 h, the current-limiting function of the SPD shall satisfy 5.2.2.2, 5.2.2.3 and 5.2.2.4.

6.2.2.6 Operating duty test

The SPD shall be connected as shown in Figure 5. The test voltage shall be the maximum interrupting voltage as specified by the manufacturer. The frequency shall be 0 (DC) or 50 Hz or 60 Hz. AC SPDs have to be tested with AC, DC SPDs have to be tested with DC, and AC/DC SPDs have to be tested with DC.

For each SPD configuration, the load current shall be adjusted (by means of the \( R_0 \), or \( R_{81} \) and \( R_{82} \) resistances) to a value selected from table 7 with the SPD temporarily replaced by a short circuit. The selected value shall be sufficient to cause the current-limiting function to operate. After the insertion of the SPD in the circuit, apply the test current until it is reduced below 10 % of the rated current.

After each SPD operation, remove the power for at least 2 min or until the current-limiting component reverts to its quiescent state. This cycle of applying test current, followed by an unpowered period, shall be repeated for the number of times indicated in table 7.

After the final cycle, the SPD shall meet the requirements of 5.2.2.2, 5.2.2.3 and 5.2.2.4.
Table 7 – Preferred values of current for operating duty tests

<table>
<thead>
<tr>
<th>Current A (d.c. or r.m.s.)</th>
<th>Applications</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5</td>
<td>60</td>
</tr>
<tr>
<td>1</td>
<td>10</td>
</tr>
<tr>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>10</td>
<td>3</td>
</tr>
</tbody>
</table>

6.2.2.7 AC durability for current limiting function

The SPD shall be connected as shown in figure 6. The a.c. short-circuit currents shall be selected from table 8. Apply currents for the specified number of applications with time between applications sufficient to prevent accumulation of heat in the device under test. The peak value of the a.c. source voltage shall not exceed the maximum interrupting voltage as specified by the manufacturer. Prior to testing and after the completion of the number of applications, the SPD shall meet the requirements of 5.2.2.1, 5.2.2.2 and 5.2.2.3.

The current shall be applied to the appropriate terminals selected from table 8. The currents may be applied to terminals X1 – X2, if it is required for three-terminal and five-terminal SPDs. For tests on three-terminal and five-terminal SPDs, each pair of terminals (X1 – C and X2 – C) on the unprotected side may be tested at the same time and same polarity, or separately.

Table 8 – Preferred values of a.c. test currents

<table>
<thead>
<tr>
<th>48-62 Hz Short-circuit currents A_{rms}</th>
<th>Duration s</th>
<th>Number of applications</th>
<th>Test terminals</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.26</td>
<td>1</td>
<td>5</td>
<td>X1 – C</td>
</tr>
<tr>
<td>0.5</td>
<td>1</td>
<td>5</td>
<td>X2 – C</td>
</tr>
<tr>
<td>0.5</td>
<td>30</td>
<td>1</td>
<td>X1 – X2</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>60</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>1</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>2.5</td>
<td>1</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>5</td>
<td></td>
</tr>
</tbody>
</table>

6.2.2.8 Impulse durability for current limiting function

The SPD shall be connected as shown in figure 7. The impulse voltages and currents shall be selected from table 9. Apply the impulse current for the specified number of applications with time between applications sufficient to prevent accumulation of heat in the device under test. Half the specified number of tests shall be carried out with one polarity followed by half with the opposite polarity. Alternatively, half of the samples may be tested with one polarity and the other half with the opposite polarity. Prior to testing and after the completion of the number of applications, the SPD shall meet the requirements of 5.2.2.1, 5.2.2.2 and 5.2.2.3.
The impulse current shall be selected from table 9 and applied to the appropriate terminals. The impulse current may be applied to terminals X1 – X2 for three-terminal and five-terminal SPDs. For tests on three-terminal and five-terminal SPDs, each pair of terminals (X1 – C and X2 – C) on the unprotected side may be tested at the same time and same polarity, or separately.

Low-current fuses may require a reduction in test \( I^t \) level to be within the SPD rating. Electronic current limiters may be designed to operate with a minimum protected load impedance or voltage (for example, a gas discharge tube in the arc mode). If required, this shall be added to the test circuit.

**Table 9 – Preferred values of impulse current**

<table>
<thead>
<tr>
<th>Open-circuit voltage</th>
<th>Short-circuit current</th>
<th>Number of applications</th>
<th>Test terminals</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 kV</td>
<td>100 A, 10/1000</td>
<td>30</td>
<td>X1 – C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>X2 – C</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>X1 – X2</td>
</tr>
<tr>
<td>1,5 kV, 10/700</td>
<td>37,5 A, 5/300</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>Maximum interrupting</td>
<td>25 A, 10/1000</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>voltage</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum interrupting</td>
<td>ITU-T Recommendation</td>
<td>10</td>
<td></td>
</tr>
<tr>
<td>voltage</td>
<td>K.44, Fig. A.3-1 (R=25Ω)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>4 kV, 1.2/50</td>
<td>2 kA, 8/20</td>
<td>10</td>
<td></td>
</tr>
</tbody>
</table>

6.2.3 Transmission tests

6.2.3.1 Capacitance

The capacitance of the SPD is measured between specified terminals at a signal generator frequency of 1 MHz and 1 V r.m.s. One pair of terminals is measured at a time; all terminals not involved in the measurement shall be connected together and grounded at the generator. No d.c. bias shall be applied. It should be noted that the capacitance of some SPDs is bias voltage dependent. In some applications this bias voltage may appear only on one line of a communications pair resulting in significant capacitance unbalance.

6.2.3.2 Insertion loss

The insertion loss in decibels is measured using leads of a maximum of 1 m in length and having the appropriate characteristic impedance. A measurement is made using the circuit of figure 8 with a short circuit replacing the SPD. The SPD is then inserted and a decibels measurement in decibels is made. The insertion loss is the vector difference between the two measurements. Table 10 lists the characteristic impedances, the frequency ranges and the cable types. The recommended test level is –10 dBm.

The measured loss of the combined baluns and test leads in figure 8 shall not exceed 3 dB within the frequency band of the transmission. The insertion loss shall be measured and recorded within the frequency band of the transmission application that the SPD is intended for use.

**Table 10 – Standard parameters for Figure 8**

<table>
<thead>
<tr>
<th>Frequency range</th>
<th>Characteristic impedance ( Z_0 ) Ω</th>
<th>Cable types</th>
</tr>
</thead>
<tbody>
<tr>
<td>300 Hz to 4 kHz</td>
<td>600</td>
<td>Twisted-pair</td>
</tr>
<tr>
<td>4 kHz to 250 MHz</td>
<td>100 or 120 or 150</td>
<td>Twisted-pair</td>
</tr>
<tr>
<td>≤ 1 GHz</td>
<td>50 or 75</td>
<td>Coaxial</td>
</tr>
<tr>
<td>&gt; 1 GHz</td>
<td>50</td>
<td>Coaxial</td>
</tr>
</tbody>
</table>
6.2.3.3 Return loss

The return loss in decibels is measured using leads of a maximum of 1 m in length and having the appropriate characteristic impedance. A measurement is made using the circuit of figure 9 with a short circuit replacing the SPD. The SPD is then inserted and a measurement in decibels is made. Table 10 lists the characteristic impedances, the frequency ranges and the cable types. The recommended test level is −10 dBm.

A signal is applied to the SPD. Signals reflected back, due to impedance discontinuities, are measured at the same terminals to which the signal is applied. The return loss shall be measured and recorded within the frequency band of the transmission application that the SPD is intended for use.

6.2.3.4 Longitudinal balance / Longitudinal conversion loss (LCL)

Longitudinal balance as calculated in the equation below is equivalent to longitudinal conversion loss (LCL) as described in ITU-T O.9 (03.1999).

Figure 10 shows the connections for longitudinal balance testing of three- four- and five-terminal SPDs. For four- and five-terminal SPDs, the test shall be carried out with switch S1 both open and closed. The longitudinal balance is the ratio of the applied longitudinal voltage $V_s$ and the resulting voltage $V_m$ of the SPD under test expressed in dB, as follows:

$$\text{Longitudinal balance (dB)} = 20 \log \left( \frac{V_s}{V_m} \right)$$

where the $V_s$ and $V_m$ signals have the same frequency.

Due to more precision at higher frequencies, a balun transformer to implement the SPD may be used instead of the shown ohmic resistances in the test set-up of Figure 10. The test bridge configuration, with transversal impedance Z1 and longitudinal impedance Z2 does not represent all conditions found in practice. Values and limits for the intended transmission characteristics, such as frequency range and voltage, special considerations for terminating impedances and measurement frequencies to be used are given in the relevant ITU-T Recommendations. An example of values and impedances for different frequency ranges up to 190 kHz is shown in Table 11. Unless otherwise specified, the test may be performed with increasing frequencies, for example at 200 Hz, 500 Hz, 1 000 Hz and 4 000 Hz for analogue applications, or at 5 kHz, 60 kHz, 160 kHz and 190 kHz for digital ISDN applications. The inherent longitudinal balance of the measuring arrangements should be 20 dB greater than the limit set for the SPD. If the longitudinal balance of the SPD is affected by the d.c. bias voltage, then the test should be carried out whilst applying the appropriate d.c. bias voltage at each SPD terminal. Requirements for the measuring arrangements are given in ITU-T Recommendation O.9.

<table>
<thead>
<tr>
<th>$f$ kHz</th>
<th>Service</th>
<th>Z1 $^a$ Ω</th>
<th>Z2 $^b$ Ω</th>
</tr>
</thead>
<tbody>
<tr>
<td>≤ 4</td>
<td>Analogue</td>
<td>300</td>
<td>150</td>
</tr>
<tr>
<td>≤ 190</td>
<td>ISDN</td>
<td>55 or 67.5</td>
<td>20-40</td>
</tr>
<tr>
<td>Up to 30 MHz</td>
<td>ADSL2+; VDSL</td>
<td>67.5</td>
<td>20-40</td>
</tr>
</tbody>
</table>

$^a$ The real difference between the test set-up and the actual longitudinal balance is somewhat independent of the terminal input impedance and therefore this analysis applies to virtually all reasonable input impedances. For details to specify Z1 and Z2, see the relevant product standard.

$^b$ Z2 should be equal to half of Z1.

Where the longitudinal conversion loss is dependent on the SPD series resistance matching, the balance may be specified as the maximum ohmic or percentage difference between the series resistances. 4
6.2.3.5 Bit Error Ratio (BER)

Bit error ratio (BER, see Figure 11), the result of dividing the number of bit errors by the total number of bits is a stream, can be used to identify the performance of a communications or data storage product. For example, 2.5 erroneous bits out of 100 000 bits transmitted would be 2.5 out of 10^5 or 2.5×10^-5. [G] Text deleted [C]

BER tests are conducted to measure the change, if any, caused by insertion of an SPD. BER tests are described in ITU-T G series (e.g. for ISDN ITU-T G.821, ADSL2 ITU-T G.992.3, VDSL ITU-T G.993.1, etc.) [G]

<table>
<thead>
<tr>
<th>Pseudo-random bit pattern, (R)</th>
<th>Duration</th>
</tr>
</thead>
<tbody>
<tr>
<td>R &lt; 64 kbits/s</td>
<td>1 h</td>
</tr>
<tr>
<td>64 kbits/s ≤ R ≤ 1 554 kbits/s</td>
<td>30 min</td>
</tr>
<tr>
<td>R ≥ 1 554 kbits/s</td>
<td>10 min</td>
</tr>
</tbody>
</table>

6.2.3.6 Near-end crosstalk (NEXT)

The crosstalk is measured on short lengths of balanced test leads terminated to the SPD according to figure 12. A balanced input signal is applied to a disturbing line of the SPD while the induced signal on the disturbed line is measured at the near end of the test leads. The recommended test signal is −10 dBm.

The measured loss of the combined baluns and test leads shall not exceed 3 dB within the frequency band of the transmission. The near-end crosstalk shall be measured and recorded within the frequency band of the transmission application that the SPD is intended for use.

6.3 Mechanical tests

6.3.1 Terminals and connectors

It shall be verified that the incorporated terminals meet the requirements of 5.3.1.

6.3.1.1 General testing procedure

The SPD is mounted according to the manufacturer’s recommendation and is protected against undue external heating or cooling.

Unless otherwise specified, the SPD terminals shall be wired with conductors using the most severe configuration (i.e., the maximum or minimum cross-sectional areas) according to

- table 13 for SPDs that have both line terminals and protected line terminals;
- the manufacturer’s instructions for other SPDs.

The SPD under test shall be fixed on a dull, black-painted wood board of about 20 mm thickness. The method of fixing shall comply with any requirements relating to the means of mounting recommended by the manufacturer. During the test, no maintenance or dismantling of the sample is allowed.

6.3.1.2 Terminals with screws

Compliance is checked by inspection and, for screws which are operated when connecting up the SPD, by the following test:

The screws are tightened and loosened

- ten times for screws in engagement with a thread of insulating material;
- five times in all other cases.
Screws or nuts in engagement with a thread of insulating material are completely removed and reinserted each time. The test is made by means of a suitable test screwdriver or spanner applying a torque as suggested by the manufacturer. The screws shall not be tightened in jerks. The conductor is removed each time the screw is loosened.

During the test, the screwed connections shall not work loose and there shall be no damage, such as breakage of screws or damage to the head slots, threads, washers or stirrups, that will impair the further use of the SPD.

Moreover, enclosures and covers shall not be damaged.

**Table 13 – Connectable cross-sectional areas of copper conductors for screw-type terminals or screwless-type terminals**

<table>
<thead>
<tr>
<th>Maximum rated current for SPDs</th>
<th>Range of nominal cross-sectional areas to be clamped</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>ISO – mm² A W G – Terminal</td>
</tr>
<tr>
<td>Up to and including 1</td>
<td>0.1 to 1 A W G – 26 to 18</td>
</tr>
<tr>
<td>Above 1 up to and including 13</td>
<td>1 to 2.5 A W G – 18 to 14</td>
</tr>
<tr>
<td>Above 13 up to and including 16</td>
<td>1 to 4 A W G – 18 to 12</td>
</tr>
</tbody>
</table>

6.3.1.3 Screwless terminals

Compliance is checked by the following tests.

The terminals are fitted with new conductors of the type and of the minimum and maximum cross-sectional areas according to table 13 for two-port SPDs or according to the manufacturer’s declaration for one-port SPDs.

Each conductor is then subjected to a pull of the value shown in table 14. The pull is applied without jerks for 1 min in the direction of the axis of the conductor.

During the test, there shall be no movement of the conductor in the terminal or any indication of damage.

**Table 14 – Pulling force (screwless terminals)**

<table>
<thead>
<tr>
<th>Cross-sectional area mm²</th>
<th>0.5</th>
<th>0.75</th>
<th>1.0</th>
<th>1.5</th>
<th>2.5</th>
<th>4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pull force N</td>
<td>30</td>
<td>30</td>
<td>35</td>
<td>40</td>
<td>50</td>
<td>60</td>
</tr>
</tbody>
</table>

6.3.1.4 Insulating pierced connections

6.3.1.4.1 Pull-out test on SPD terminals designed for single-core conductors

Compliance is checked by the following tests.

The terminals are fitted with new copper conductors of the smallest or largest cross-sectional area specified in 6.3.1.1, solid or stranded, whichever is most unfavourable. Screws, if any, are tightened as suggested by the manufacturer.
The conductors are connected and disconnected five times, new conductors being used each time. After each connection, the conductors are subjected to a pull, without jerks, for 1 min in the axis of the conductor according to the value given in table 14.

During the test, there shall be no movement of the conductor in the terminal or any sign of damage.

6.3.1.4.2 Pull-out test on SPD terminals designed for multi-core cables or cords

The pull-out test on the SPD terminals designed for multi-core cables or cords is carried out according to 6.3.1.4.1 except that the pull force is applied to the entire multi-core cable or cord instead of the individual core.

The pull force is calculated according to the following formula:

\[ F = F(x) \sqrt{n} \]

where

- \( F \) is the total force to be applied;
- \( n \) is the number of cores;
- \( F(x) \) is the force for one core according to the cross-sectional area of one conductor (see table 14).

During the test the cable or cord shall not slip out of the terminals.

6.3.2 Mechanical strength (mounting)

It shall be verified by inspection that SPDs have adequate mechanical strength to withstand the stresses imposed during installation and use.

6.3.3 Resistance to ingress of solid objects and to harmful ingress of water

Test in accordance with IEC 60529 to check the IP code.

6.3.4 Protection against direct contact

Insulating parts

The sample is mounted as for normal use and fitted with conductors of the smallest cross-sectional areas and the test is repeated using conductors of the largest cross-sectional areas (see table 13). The standard test finger (in accordance with IEC 60529) is applied in every possible position.

For plug-in SPDs (which can be changed without a tool), the test finger is applied in every possible position, when the plug is partially engaged or completely engaged with a socket outlet. An electrical indicator with a voltage of not less than 40 V and not more than 50 V, is used to show contact with the relevant part.

Metal parts

Metal parts which are accessible when the SPD is wired and mounted as for normal use shall be connected to ground through a low-resistance connection, except for small screws and the like, insulated from live parts, for fixing bases and covers or cover plates of socket-outlets.
A current (derived from an a.c. source having a no-load voltage not exceeding 12 V) equal to
1.5 times the rated current or to 25 A, whichever is the greater, is passed between the
grounding terminal and each of the accessible metal parts in turn.

The voltage drop between the grounding terminal and the accessible metal part is measured
and the resistance is calculated from the current and this voltage drop. The resistance shall
not exceed 0.05 Ω.

NOTE Care should be taken that the contact resistance between the tip of the measuring probe and the metal
part under test does not influence the test results.

6.3.5 Fire resistance

The glow-wire test is performed in accordance with clauses 4 to 10 of IEC 60695-2-1/1 under
the following conditions:

- for external parts of SPD made of insulating material necessary to retain in position
current-carrying parts and parts of the protective circuit, by the test made at a temperature
of 850 °C ± 15 °C;
- for all other external parts made of insulating material, by the test made at a temperature
of 650 °C ± 10 °C.

For the purposes of this test, bases of surface-type SPDs are considered as external parts.
The test is not made on parts of ceramic material. If the insulating parts are made of the same
material, the test is carried out only on one of these parts, at the appropriate glow-wire test
temperature.

The glow-wire test is applied to ensure that an electrically heated test wire under defined test
conditions does not cause ignition of insulating parts, or to ensure that a part of insulating
material, which might be ignited by the heated test wire under defined conditions, has a
limited time to burn without spreading fire by flame or burning parts or droplets falling from the
tested part.

The test is made on one sample. In case of doubt, the test is repeated on two further
samples. The test is made by applying the glow-wire once. The sample shall be positioned
during the test in the most unfavourable position of its intended use (with the surface tested in
a vertical position).

The tip of the glow-wire shall be applied to the specified surface of the test sample taking into
account the conditions of intended use under which a heated or glowing element may come
into contact with the sample.

The sample is regarded as having passed the glow-wire test if

- there is no visible flame and no sustained glowing, or if
- flames and glowing on the sample extinguish themselves with 30 s after the removal of the
glow-wire.

There shall be no ignition of the tissue paper or scorching of the pine wood board.
6.4 Environmental tests

6.4.1 High temperature and humidity endurance

The SPD shall be exposed to high temperature and relative humidity conditions for a duration selected from table 15. The temperature shall be 80 °C +/- 2K. The relative humidity shall be between 90% and 96%.

The SPD shall be tested using the appropriate test circuit of figure 13. The SPD shall be powered with a d.c. or a.c. supply throughout the exposure. The power supply voltage shall be equal to the maximum continuous operating voltage specified in 5.2.1.1. This power supply shall have sufficient current capability to supply the current drawn by the SPD under test. After the exposure, the SPD shall be cooled to an ambient temperature of 23 °C ± 2 °C.

Table 15 – Preferred values of test-time duration for high temperature and humidity endurance

<table>
<thead>
<tr>
<th>Test-time duration</th>
<th>Days</th>
</tr>
</thead>
<tbody>
<tr>
<td>10</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td></td>
</tr>
<tr>
<td>56</td>
<td></td>
</tr>
</tbody>
</table>

6.4.2 Environmental cycling with impulse surges

The SPD shall be exposed to the non-condensing environmental cycle for the duration corresponding to the cycle selected from table 16. During the exposure, a generator of impulses having the characteristics specified in table 3 shall be used to apply sufficient open-circuit voltage selected from Category C of table 3.

When cycle A is selected, two impulse currents shall be applied each cycling day for five consecutive days, followed by two days without application. Alternatively, when cycle B is selected two impulse currents shall be applied at the first day and the last day of the temperature cycling. On each surge day, one impulse current is applied at high extreme temperature $T_1$, given in Table 16, and the other at low extreme temperature $T_2$, given in Table 16. The surges shall be applied within 1h of the centre of the dwell time at low and high extreme temperatures. The impulse currents on a given day shall be of the same polarity, but shall alternate polarity on the next test day. This procedure shall be repeated until the completion of the environmental cycling.

The SPD shall be tested using the appropriate test circuit of figure 13 and shall be powered with a d.c. supply throughout the environmental cycling. The negative or positive level of the d.c. power supply shall not exceed the rated voltage specified in 5.2.1.1. The SPD shall not be powered with the d.c. power supply during the application of the impulse current.
Table 16 – Preferred values of temperature and duration for environmental cycling tests

<table>
<thead>
<tr>
<th>Cycle</th>
<th>High extreme temperature ( (T_1) ) °C</th>
<th>Low extreme temperature ( (T_2) ) °C</th>
<th>Duration cycles</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cycle A – Figure 14</td>
<td>32 ± 2</td>
<td>4 ± 2</td>
<td>30</td>
</tr>
<tr>
<td>Cycle B – Figure 15 (based on IEC 60068-2-30; 6.3.3, variant 2)</td>
<td>40 or 55 ± 2</td>
<td>25 ± 3</td>
<td>5</td>
</tr>
</tbody>
</table>

The impulse-limiting voltage shall be measured during the application of each impulse current. The insulation resistance shall be measured within 1 h after each surge application. If the SPD is known to be sensitive to the polarity of the d.c. power supply, it shall be tested for insulation resistance with positive and negative polarities.

Within 1 h after the end of the environmental cycling, the SPD shall satisfy the requirements of 5.2.1.2 and 5.2.1.3.

### 6.4.3 Environmental cycling with a.c. surges

The SPD shall be exposed to the non-condensing environmental cycle for the duration corresponding to the cycle selected from table 16. During the exposure, using a generator, apply sufficient open-circuit a.c. voltage with short-circuit current selected from table 5.

When cycle A is selected, two impulse currents shall be applied each cycling day for five consecutive days followed by two days without application. Alternatively, when cycle B is selected, two impulse currents shall be applied at the first day and the last day of the temperature cycling. On each surge day, one impulse current is applied at high extreme temperature \( T_1 \), given in Table 16, and the other at low extreme temperature \( T_2 \) given in Table 16. The surges shall be applied within 1 h of the centre of the dwell time at low and high extreme temperatures. The a.c. surges shall be applied within 1 h of the centre of the dwell time at low and high extreme temperatures. This procedure shall be repeated until the completion of the environmental cycling.

The SPD shall be tested using the appropriate test circuit of figure 13 and shall be powered with a d.c. supply throughout the environmental cycling. The negative or positive level of the d.c. power supply shall not exceed the rated voltage determined in 5.2.1.1. The SPD shall not be powered with the d.c. power supply during the application of the a.c. current.

The a.c. limiting voltage shall be measured during the application of each current. The insulation resistance shall be measured within 1 h after each a.c. surge application. If the SPD is known to be sensitive to the polarity of the d.c. power supply, it shall be tested for insulation resistance with positive and negative polarities.

Within 1 h after the end of the environmental cycling, the voltage-limiting function shall satisfy the impulse-limiting voltage and the insulation resistance requirements.

### 6.5 Acceptance tests

Acceptance tests are made by agreement between the manufacturer and user.
Key

- **O, O₁, O₂**: oscilloscopes
- **E, E₁, E₂**: DC or AC voltage sources
- **G**: impulse generator
- **IE**: isolation element
- **$R_{S1}, R_{S2}$**: non-inductive source resistors
- **$D, D_1, D_2$**: diodes are used at DC sources, decoupling elements are used at AC sources
- **V**: voltage-limiting component
- **V, I**: voltage-limiting components or combination of voltage-limiting and current-limiting components
- **X₁, X₂**: line terminals
- **Y₁, Y₂**: protected line terminals
- **C**: Common terminal

**Figure 2** – Test circuits for impulse reset time
Key:

A, A₁, A₂  ammeters  V  voltage-limiting component
E  a.c. voltage source  V, I  voltage-limiting components or combination of
R₂, R₅₁, R₅₂  non-inductive source resistors  voltage-limiting and current-limiting components

X₁, X₂  line terminals
Y₁, Y₂  protected line terminals
C  common terminal

Figure 3 – Test circuits for a.c. durability and overstressed fault mode
Figure 4 – Test circuits for impulse durability and overstressed fault mode
Figure 5 – Test circuits for rated current, series resistance, response time, current reset time, maximum interrupting voltage and operating duty test
Key
A, A₁, A₂ ammeters
E a.c. voltage source
R₀, Rₜ₁, Rₜ₂ non-inductive source resistors
V voltage-limiting component
V, I voltage-limiting components or combination of voltage-limiting and current-limiting components
X₁, X₂ line terminals
Y₁, Y₂ protected line terminals
C common terminal

Figure 6 – Test circuits for a.c. durability
Key

O, O₁, O₂  oscilloscopes
G    impulse generator
V    voltage-limiting component
V, I  voltage-limiting components or combination of voltage-limiting and current-limiting components
X₁, X₂  line terminals
Y₁, Y₂  protected line terminals
C    common terminal

Figure 7 – Test circuits for impulse durability
Figure 8 – Test circuits for insertion loss

Figure 9 – Test circuit for return loss
Key

- $V_s$: disturbing common mode (longitudinal) voltage
- $V_m$: resulting differential mode (metallic) voltage
- $Z_1, Z_2$: terminating impedance

- $V$: voltage-limiting component
- $V, I$: voltage-limiting components or combination of voltage-limiting and current-limiting components
- X1, X2: line terminals
- Y1, Y2: protected line terminals
- C: common terminal

Figure 10 – Test circuits for longitudinal balance
Figure 11 – Test circuit for bit error ratio test
Key
N  network analyser
B  balun
Z1, Z2 terminating impedances

Figure 12 – Test circuit for near-end crosstalk
Figure 14 – Environmental cycling schedule A with RH ≥ 90%
Figure 15 – Environmental cycling B

Key

$T_1$  upper temperature, $+40$ °C or $+55$ °C

$t_1$  end of the temperature rise

$t_2$  start of the temperature fall

$T_1 + 2$ °C

$T_1 - 2$ °C

$+28$ °C

$+22$ °C

$25$ °C

$\pm 0.5$ h

$3$ h

$12$ h $\pm 0.5$ h

$24$ h

$3$ h

$6$ h
Star protection circuit

Diode steering bridge

Key

<table>
<thead>
<tr>
<th>Line terminals</th>
<th>Protected line terminals</th>
<th>Common</th>
</tr>
</thead>
<tbody>
<tr>
<td>X1, X2, Xn</td>
<td>Y1, Y2, Yn,</td>
<td>C</td>
</tr>
</tbody>
</table>

1 Individual protective element
2 Common protective element

Figure 16 – Examples of multi-terminal SPDs with a common current path
Annex A
(informative)

Devices with current-limiting components only

Configurations of devices with current-limiting components only are shown in figure A.1. Such a device should be tested to the applicable requirements of 5.2.2. The voltage source used in the tests of 6.2.2 shall have a value that is less than or equal to the maximum interrupting voltage as specified by the manufacturer. The current protective device shall also be subjected to the tests of 6.3 and selected tests in 6.2.3, depending on its application.

Figure A.1a – Two-terminal current-limiter
Figure A.1b – Three-terminal current-limiter
Figure A.1c – Four-terminal current-limiter
Figure A.1d – Five-terminal current-limiter

Key
- I: current-limiting-component(s)
- X1, X2: line terminals
- Y1, Y2: protected line terminals
- C: common terminal

Figure A.1 – Configurations of devices with current-limiting component(s) only
Annex B

Annex deleted
Annex C

Annex deleted
IEC 61083-1 defines the measurement accuracy for analogue type and digital type impulse recorders, such as a digital oscilloscope with probes. Analogue recorders shall have rise times five times faster than the signal rise time. This ensures less than 2 % error in the displayed rise time. Digital recorders shall have sample times at least 30/TX where TX is the time interval to be measured. A rated resolution of 0.4 % of full-scale deviation (2^-8 full-scale deviation) or better is recommended for tests where only the impulse parameters are to be evaluated. For reference tests, which require comparison of records, a rated resolution of 0.2 % of full-scale deviation (2^-9 full-scale deviation) or better shall be used. IEC 61083-1 also covers additional accuracy parameters for specific waveshapes.
Annex E
(informative)

Determination of let-through current ($I_p$)

To determine the maximum let-through current $I_p$ at the output terminals of an SPD, the input terminals should be exposed to a specified test impulse selected from Table 3. The output current waveform into a short-circuit (Figures E.1 to E.6) should be measured. If the measured waveform is equal to the waveform given by Table 3, than the value $I_p$ is given by the peak value of the measured current. Where the measured waveform deviates from the specified waveform according to Table 3, it can be assumed that at Figures 1b to 1f, the measured maximum current corresponds to $I_p$. At Figure 1a, $I_p$ is equal to the short-circuit current of the generator. To get an exact calculation of coordination, it is necessary to use the let-through energy (LTE) method (see Clause F.5 of IEC 61643-12 or Clause C.4 of IEC 62305-4).

This determination of the let-through current ($I_p$) is used to calculate a coordination of SPDs (see Figure E.1 in IEC 61643-22).

If several test impulses are specified, the maximum values of $U_p$ and $I_p$ should be indicated for each test impulse. Depending on the type of SPD (see 1.2), the test a), b) or c) should be chosen.

a) Asymmetrical application of test impulses to determine the differential mode $I_p$ (see Figure E.1). The test impulse is applied to the input side of the SPD.

b) Non-symmetrical application of test impulses to determine the common mode $I_p$ (see Figure E.2). The test impulse is applied to the input side of the SPD.

c) Symmetrical application of test impulses to determine the differential mode $I_p$ (see Figure E.3). The test impulse is applied by a current distributor (1:2) to the input side of the SPD.

d) Asymmetrical application of test impulses to determine the differential mode $I_p$ (see Figure E.4). The test impulse is applied to the input side of the SPD.

e) Symmetrical application of test impulses to determine the common mode $I_p$ (see Figure E.5). The test impulse is applied by a current distributor (1:2) to the input side of the SPD.

f) Symmetrical application of test impulses to determine the common mode $I_p$ (see Figure E.6). The test impulse is applied by a current distributor (1:n) to the input side of the SPD.

NOTE: The value of $I_p$ is equal to the surge current of the generator.

Figure E.1 – Determination of differential mode let-through current

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Figure E.2 – Determination of common mode let-through current

Figure E.3 – Determination of differential mode let-through current

Figure E.4 – Determination of differential mode let-through current

Figure E.5 – Determination of common mode max. let-through current
Figure E.6 – Determination of common mode max. let-through current at multi-terminal SPDs

IEC 663/08
Annex F
(informative)

Basic configurations for measuring $U_p$

NOTE 1 XA and XB are the surge generator connections, which are sequentially connected to the terminal pairs formed by X1, X2 through to Xn.

NOTE 2 YA and YB connect to the associated Y terminal pair of the tested X terminal pair to measure $U_p$.

NOTE 3 ------ Possible link to C terminal used for ITU-T test setups.

Figure F.1 – Differential Mode $U_p$ measurement of Figure 1 SPDs

NOTE 4 R1 through Rn are impulse current sharing resistors (may be internal or external)

Figure F.2 – ITU-T test setup for SPD Common Mode $U_p$ measurement to C terminal
Annex G
(informative)

Special resistibility in telecommunication systems

Special resistibility may be required when mains SPDs cannot be installed and when bonding between the mains and telecommunication systems cannot be achieved.

For example, ITU-T K.44 requires a B2 impulse with an open circuit voltage of 13 kV and a short-circuit current of 325 A. 📌
Bibliography


IEC 60068-1:1988, Environmental testing – Part 1: General and guidance


IEC 60664-1, Insulation coordination for equipment within low-voltage systems – Part 1: Principles, requirements and tests

NOTE Harmonised as EN 60664-1

IEC 60664-2-1:2011, Insulation coordination for equipment within low-voltage systems – Part 2-1: Application guide – Explanation of the application of the IEC 60664 series, dimensioning examples and dielectric testing

IEC 60721-3-3:1994, Classification of environmental conditions – Part 3: Classification of groups of environmental parameters and their severities – Section 3: Stationary use at weatherprotected locations

IEC 61180-1, High-voltage test techniques for low-voltage equipment – Part 1: Definitions, test and procedure requirements


ITU-T Recommendation K.20:1996, Resistibility of telecommunication switching equipment to overvoltages and overcurrents

ITU-T Recommendation K.21:1996, Resistibility of subscriber’s terminals to overvoltages and overcurrents


ITU-T K.44:2003, Resistibility tests for telecommunication equipment exposed to overvoltages and overcurrents – Basic recommendation

ITU-T Recommendation K.45:2008, Resistibility of telecommunication equipment installed in the access and trunk networks to overvoltages and overcurrents

ITU-T Recommendation K.65:2011, Overvoltage and overcurrent requirements for termination modules with contacts for test ports or surge protective devices
## Normative references to international publications with their corresponding European publications

The following referenced documents are indispensible for the application of this document. For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments) applies.

**NOTE** Where an International Publication has been modified by common modifications, indicated by (mod), the relevant EN/HD applies.

<table>
<thead>
<tr>
<th>Publication</th>
<th>Year</th>
<th>Title</th>
<th>EN/HD</th>
<th>Year</th>
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<tbody>
<tr>
<td>IEC 60050-702</td>
<td>1992</td>
<td>International Electrotechnical Vocabulary (IEV) - Chapter 702: Oscillations, signals and related devices</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>IEC 60050-726</td>
<td>1982</td>
<td>International Electrotechnical Vocabulary (IEV) - Chapter 726: Transmission lines and waveguides</td>
<td>-</td>
<td>-</td>
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<tr>
<td>IEC 60060-1</td>
<td>1989</td>
<td>High-voltage test techniques - Part 1: General definitions and test requirements</td>
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²) Undated reference.

³) Valid edition at date of issue.


⁵) EN 60950:2000 is superseded by EN 60950-1:2006 "Information technology equipment - Safety - Part 1: General requirements", which is based on IEC 60950-1:2005, modified.
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